IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A liquid crystal display comprising:

a pixel array portion having signal lines and scanning lines horizontally and vertically aligned, and pixel transistors formed in the vicinity of each intersection of said signal line and said scanning line;

a plurality of first latch circuits configured to latch digital gradation data consisting of a plurality of bits in different timings;

a plurality of second latch circuits which are provided in accordance with each of a plurality of said first latch circuits and latch data latched by each of a plurality of said first latch circuits at the same time;

a plurality of D/A converters which are provided in accordance with each of a plurality of second latch circuits and convert latch data latched by each of a plurality of said second latch circuits into analog gradation voltage; and

a signal line selection circuit configured to switch whether said analog gradation voltage is supplied to each signal line so that said signal lines in said pixel array portion are driven every multiple signal lines in multiple times.

Claim 2 (Original): The liquid crystal display according to claim 1, wherein said signal line selection circuit has a plurality of analog switches which are provided in accordance with each of said signal lines and switch whether said analog gradation voltage is supplied to a corresponding signal line; and

said signal line selection circuit controls a plurality of said analog switches to be turned on/off so that said signal lines are driven every multiple signal lines in multiple times.

Claim 3 (Original): The liquid crystal display according to claim 2, wherein said first latch circuits, said second latch circuits, said D/A converters and said analog switches are formed on the same insulating substrate as said signal lines, said scanning lines and said pixel transistor; and

a plurality of said analog switches are provided in accordance with each of said D/A converters and a plurality of said analog switches are sequentially turned on one by one.

Claim 4 (Original): The liquid crystal display according to claim 2, wherein assuming that an aggregate number of said signal lines is n (n is an integer not less than 2), n/m sets ($2 \leqq m < n/2$, and n/m is an integer) of said first latch circuits, said second latch circuits and said D/A converters are provided; and

m pieces of analog switches are provided for each of said D/A converters.

Claim 5 (Original): The liquid crystal display according to claim 4, wherein said first latch circuit includes a digital gradation data supply circuit configured to supply digital gradation data for said first latch circuit; and

said digital gradation data supply circuit sequentially supplies said digital gradation data corresponding to every m-th signal line to said first latch circuit.

Claim 6 (Original): The liquid crystal display according to claim 1, wherein said first latch circuit includes a first level conversion circuit configured to convert digital gradation data into digital gradation data in a first voltage range.

Claim 7 (Original): The liquid crystal display according to claim 1, further comprising a second level conversion circuit which is inserted between said second latch

circuit and said D/A converter and converts digital gradation data outputted from said second latch circuit into digital gradation data in a second voltage range,

wherein said D/A converter performs conversion into an analog gradation voltage based on an output from said second level conversion circuit.

Claim 8 (Original): The liquid crystal display according to claim 1, wherein said D/A converter includes:

a decoder configured to decode an output from said second latch circuit; and

a plurality of analog switches which are controlled to be turned on/off in accordance with a decoding result by said decoder and to which analog gradation voltages on different voltage levels are supplied at each one end,

said signal selection circuit supplying to a corresponding signal line said analog gradation voltage fed to one end of said analog switch turned on in accordance with a decoding result by said decoder.

Claim 9 (Original): The liquid crystal display according to claim 1, wherein said D/A converter includes:

a plurality of resistance devices connected between a first voltage terminal and a second voltage terminal in series; and

a selection circuit configured to select and supply any one of voltages at respective connection points of a plurality of said resistance devices to a corresponding signal line based on an output from said second latch circuit,

voltages on different voltage levels being supplied from the outside of said insulating substrate to said first and second voltage terminals.

Claim 10 (Original): The liquid crystal display according to claim 9, further comprising a plurality of electric current amplification circuits connected to said respective connection points of a plurality of said resistance devices,

wherein said selection circuit selects any one of outputs from said electric current amplification circuits based on an output from said second latch circuit.

Claim 11 (Original): The liquid crystal display according to claim 1, further comprising a shift register configured to output a latch timing signal of each of a plurality of said first latch circuits,

wherein a plurality of said second latch circuits carry out the latch operation based on a load signal generated by an output from said shift register.

Claim 12 (Original): The liquid crystal display according to claim 1, wherein said signal line selection circuit selects all signal lines corresponding to either odd-numbered pixels or even-numbered pixels in a first half of a one-horizontal-line display period, and selects all signal lines corresponding to the other of odd-numbered pixels or even-numbered pixels in a last half of a one-horizontal-line display period.

Claim 13 (Currently Amended): The liquid crystal display according to claim 12, wherein said D/A converter performs conversion into an analog gradation voltage based on a reference voltage whose voltage level differs in accordance with a case where said signal line selection circuit selects a signal line corresponding to odd-numbered pixels and a case where said signal line selection circuit selects a signal line corresponding to even-numbered pixels.

Claim 14 (Currently Amended): A data latch circuit comprising:

a memory circuit which has first and second inverters having one output terminal connected to the other input terminal and the other output terminal connected to one input terminal and stores therein digital data which is a latch target;

first and second switch devices configured to switch and controlling whether a power supply voltage is supplied to said first and second inverters;

a third switch device configured to switch and controlling whether said digital data is inputted to said memory circuit; and

an output circuit configured to read digital data stored in said memory circuit,

said first and second switch devices being turned on in a period other than a cyclic sampling period to supply a power supply voltage to said first and second inverters,

said third switch device being turned on in said sampling period to input digital data to said memory circuit,

said output circuit having a passing electric current prevention ~~function so as not to cause~~ unit which prevents a passing electric current to flow from a power supply terminal of said output terminal to a group terminal in said sampling period.

Claim 15 (Original): The data latch circuit according to claim 14, wherein said output circuit outputs a signal having predetermined logic in said sampling period, and inverts and outputs data stored in said memory circuit in a period other than said sampling period.

Claim 16 (Original): The data latch circuit according to claim 15, wherein said output circuit includes:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter in a period other than said sampling period.

Claim 17 (Original): The data latch circuit according to claim 16, wherein said first and second logical operation circuits include any one of an NAND gate, an NOR gate and a clocked inverter.

Claim 18 (Original): The data latch circuit according to claim 15, wherein to said output circuit are supplied a first signal indicating whether or not to be said sampling period and a second signal which has specific logic in a predetermined period other than said sampling period, and

said output circuit including:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter when said second signal has said specific logic in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter when said second signal has said specific logic in a period other than said sampling period.

Claim 19 (Original): The data latch circuit according to claim 18, wherein said first and second logical operation circuits include any one of an NAND gate, an NOR gate and a clocked inverter.

Claim 20 (Currently Amended): A liquid crystal display comprising:

signal lines and scanning lines being aligned;

display elements arranged in the vicinity of an intersection of said signal line and said scanning line;

a signal line drive circuit configured to drive each of said signal lines; and

a scanning line drive circuit configured to drive each of said scanning lines,

said signal line dive circuit including:

a shift register which has a plurality of register circuits and sequentially outputs shift register shift pulses shifted in synchronization with a clock signal;

a plurality of data latch circuits configured to latch digital data concerning pixel information in synchronization with each of said shift pulses;

a load latch circuit configured to simultaneously latch outputs from a plurality of said data latch circuits in synchronization with a load signal; and

a D/A converter circuit configured to convert a latch output from said load latch circuit into an analog pixel voltage to be then supplied to a corresponding signal line,

each of a plurality of said data latch circuits including:

a memory circuit which has first and second inverters having one output and being connected to the other input terminal and the other output terminal being connected to one input terminal, and stores therein digital data which is a latch target;

first and second switch devices configured to switch and controlling whether a power supply voltage is supplied to said first and second inverters;

a third switch device configured to switch and controlling whether said digital data is inputted to said memory circuit; and

an output circuit configured to read digital data stored in said memory circuit,

said first and second switch devices being turned on in a period other than a cyclic sampling period to supply a power supply voltage to said first and second inverters,

said third switch device being turned on in said sampling period to input digital data to said memory circuit,

said output circuit having a passing electric current prevention ~~function so as not to cause~~ unit which prevents a passing electric current to flow from a power supply terminal of said output terminal to a group terminal in said sampling period.

Claim 21 (Original): The data latch circuit according to claim 20, wherein said output circuit includes:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter in a period other than said sampling period,

said first and second logical operation circuits being constituted by circuits which are equivalent to each other.